

**16-Bit D-Type Flip-Flop
with 3-STATE Outputs**

Product Features

- The PI74VCX Family is designed for low voltage operation, $V_{DD} = 1.8V$ to $3.6V$
- 3.6V I/O Tolerant Inputs and Outputs
- Supports Live Insertion
- Balanced Drive, $\pm 24mA$
- Uses patented Noise Reduction Circuitry
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{DD} = 2.5V$, $T_A = 25^\circ C$
- Typical V_{OHV} (Output V_{OH} Undershoot) $< -0.6V$ at $V_{DD} = 2.5V$, $T_A = 25^\circ C$
- Power-Off high impedance inputs and outputs
- Industrial operation at $-40^\circ C$ to $+85^\circ C$
- Packages available:
 - 48-pin 240 mil. wide plastic TSSOP (A)
 - 48-pin 300 mil. wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74VCX series of logic circuits are produced in the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

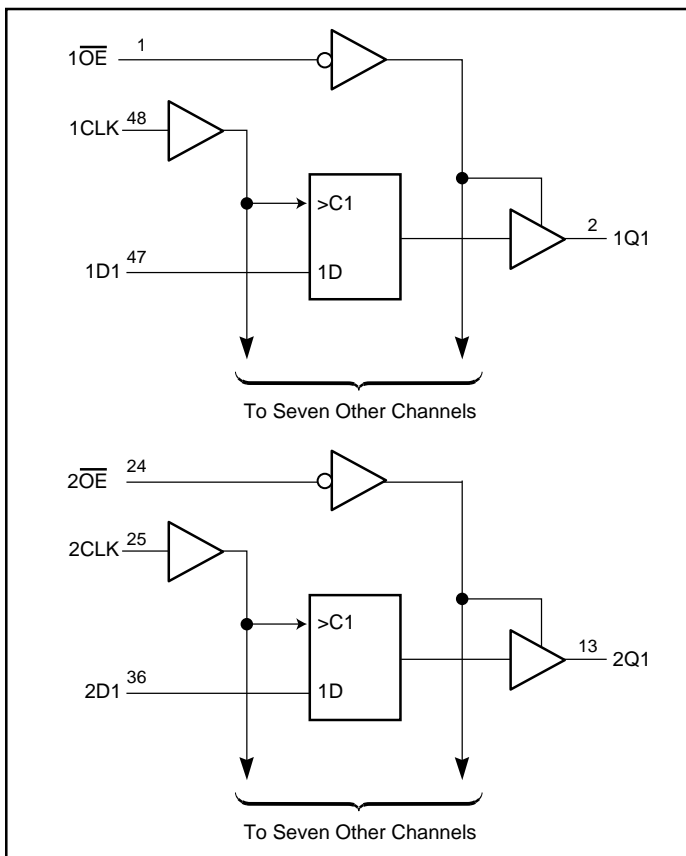
The PI74VCX16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit Flip-Flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered Output Enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state in which the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74VCX family is I/O Tolerant, allowing it to operate in mixed 1.8V/3.6V systems.

Logic Block Diagram



Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW)
CLK	Clock Input
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
Vcc	Power

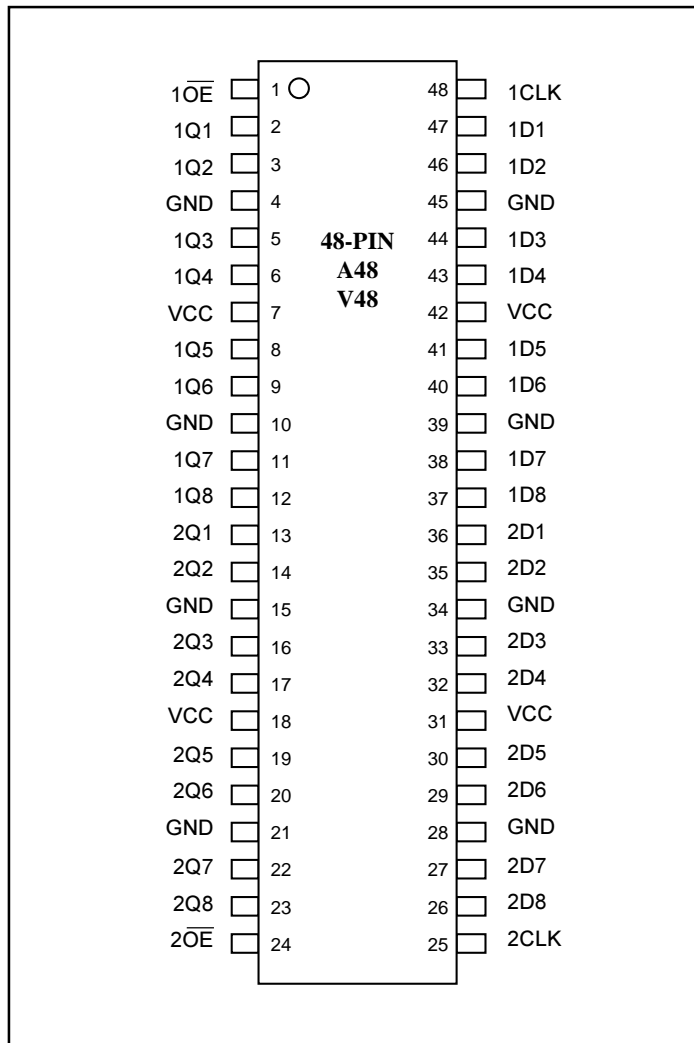
Truth Table⁽¹⁾

Inputs			Outputs
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

Notes:

- H = High Signal Level
 L = Low Signal Level
 X = Don't Care or Irrelevant
 Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD}	-0.5V to 4.6V
Input Voltage Range, V_I	-0.5V to 4.6V
Output Voltage Range, V_O (3-States)	-0.5V to 4.6V
Output Voltage Range, $V_O^{(1)}$ (Active)	-0.5V to $V_{DD} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50mA
$V_O > V_{DD}$	-50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	$\pm 50mA$
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND)	$\pm 100mA$
Storage Temperature Range, T_{STG}	-65°C to 150°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions⁽²⁾

Parameters	Description	Conditions	Min.	Max.	Units
V_{DD}	Supply voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	$V_{DD} = 2.7V$ to $3.6V$	2.0		
V_{IL}	Low-level input voltage	$V_{DD} = 2.7V$ to $3.6V$		0.8	
V_I	Input voltage		-0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	$V_{DD} = 3.0V$ to $3.6V$ $V_{DD} = 2.3V$ to $2.7V$ $V_{DD} = 1.8V$		± 24 ± 18 ± 6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate ⁽³⁾		0	10	ns/V
T_A	Operating free-air temperature		-40	85	C

Notes:

1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
- 3 As measured between 0.8V and 2.0V, $V_{DD} = 3.0V$.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics (2.7V < V_{DD} ≤ 3.6V)

Parameters	Description	Conditions	V _{DD}	Min.	Typ.	Max.	Units
V _{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0			V
V _{IL}	LOW Level Input Voltage					0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100μA		V _{DD} - 0.2			
		I _{OH} = -12mA	2.7	2.2			
		I _{OH} = -18mA	3.0	2.4			
		I _{OH} = -24mA		2.2			
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA	2.7 - 3.6			0.2	
		I _{OL} = 12mA	2.7			0.4	
		I _{OL} = 18mA	3.0			0.4	
		I _{OL} = 24mA				0.5	
I _I	Input Leakage Current	V _I = 0.0V, V _I = 3.6V	3.6			±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.7 - 3.6			±10	
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0			10	
I _{DD}	Quiescent Supply Current	V _I = V _{DD} to GND	2.7 - 3.6			20	
		V _{DD} ≤ (V _I , V _O) ≤ 3.6V				±20	
ΔI _{DD}	Increase in I _{DD} per input	V _{IH} = V _{DD} - 0.6V, Other inputs at V _{DD} or GND				750	

DC Characteristics (2.3V ≤ V_{DD} ≤ 2.7V)

Parameters	Description	Conditions	V _{DD}	Min.	Typ.	Max.	Units
V _{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.6			V
V _{IL}	LOW Level Input Voltage			V _{DD} - 0.2		0.7	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100μA		2.3	2.0		
		I _{OH} = -6mA		1.8			
		I _{OH} = -18mA		1.7			
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA	2.3 - 2.7			0.2	
		I _{OL} = 12mA	2.3			0.4	
		I _{OL} = 18mA				0.4	
I _I	Input Leakage Current	V _I = 0.0V, V _I = 2.7V	2.7			±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.3 - 2.7			±10	
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0			10	
I _{DD}	Quiescent Supply Current	V _I = V _{DD} or GND	2.3 - 2.7			20	
		V _{DD} ≤ (V _I , V _O) ≤ 3.6V				±20	

DC Characteristics (1.8V ≤ V_{DD} ≤ 2.3V)

Parameters	Description	Conditions	V _{DD}	Min.	Typ.	Max.	Units
V _{IH}	HIGH Level Input Voltage		1.8 - 2.3	0.7 x V _{DD}			V
V _{IL}	LOW Level Input Voltage			0.2 x V _{DD}			
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100μA	1.8	V _{DD} - 0.2			
		I _{OH} = -6mA		1.4			
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA					0.2
		I _{OL} = 6mA					0.3
I _I	Input Leakage Current	V _I = 0.0V, V _I = 1.8V				±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}				±10	
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0			10	
I _{DD}	Quiescent Supply Current	V _I = V _{DD} or GND	1.8			20	
		V _{DD} ≤ (V _I , V _O) ≤ 3.6V	1.8			±20	

Note:

1. Not guaranteed

AC Electrical Characteristics

Symbol	Parameters	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$						Units
		$V_{DD} = 3.3\text{V} \pm 0.3\text{V}$		$V_{DD} = 2.5\text{V} \pm 0.2\text{V}$		$V_{DD} = 1.8\text{V}$		
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	250		250		250		MHz
$t_{\text{PLH}}, t_{\text{PHL}}$	Prop Delay, CLK to Q	0.8	3.0	1.0	3.9	1.5	6.0	ns
$t_{\text{pZH}}, t_{\text{pZL}}$	Output Enable Time	0.8	3.5	1.0	4.6	1.5	7.0	
$t_{\text{pHZ}}, t_{\text{pLZ}}$	Output Disable Time	0.8	3.5	1.0	3.8	1.5	5.0	
$t_{\text{OSHL}}, t_{\text{OSLH}}$	Output to Output Skew ⁽²⁾		0.5		0.5		0.5	

Notes:

- For $C_L = 50\text{pF}$ add approximately 300ps to AC maximum specification.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

AC Setup Requirements

Symbol	Parameters	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$						Units
		$V_{DD} = 3.3\text{V} \pm 0.3\text{V}$		$V_{DD} = 2.5\text{V} \pm 0.2\text{V}$		$V_{DD} = 1.8\text{V}$		
		Min.	Typ.	Min.	Typ.	Min.	Typ.	
t_{SU}	Setup Time	1.5		1.5		2.5		ns
t_{H}	Hold Time	1.0		1.0		1.0		
t_{W}	Pulse Width	1.5		1.5		3.0		

Dynamic Switching Characteristics

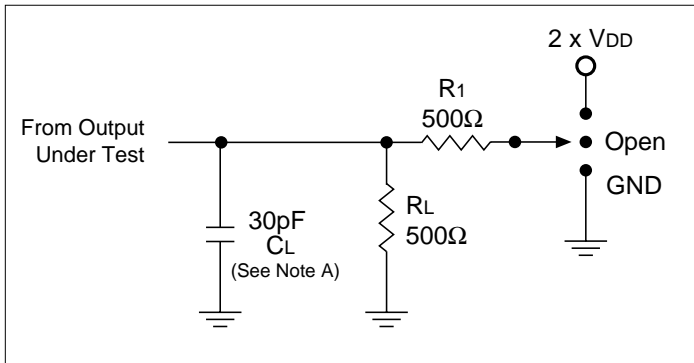
Symbol	Parameters	Conditions	V_{DD}	$T_A = +25^\circ\text{C}$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{pF}$ $V_{\text{IH}} = V_{\text{DD}}$ $V_{\text{IL}} = 0\text{V}$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLP}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{pF}$ $V_{\text{IH}} = V_{\text{DD}}$ $V_{\text{IL}} = 0\text{V}$	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V_{OLP}	Quiet Output Dynamic Valley V_{OH}	$C_L = 50\text{pF}$ $V_{\text{IH}} = V_{\text{DD}}$ $V_{\text{IL}} = 0\text{V}$	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameters	Conditions	$T_A = +25^\circ\text{C}$ Typical	Units
C_{IN}	Input Capacitance	$V_{\text{DD}} = 1.8, 2.5\text{V or } 3.3\text{V}, V_{\text{I}} = 0\text{V or } V_{\text{DD}}$	6	pF
C_{OUT}	Output Capacitance	$V_{\text{I}} = 0\text{V or } V_{\text{DD}}, V_{\text{DD}} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	7	
C_{PD}	Power Dissipation Capacitance	$V_{\text{I}} = 0\text{V or } V_{\text{DD}}, F = 10\text{ MHz}$ $V_{\text{DD}} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	20	

Test Circuits and Switching Waveforms

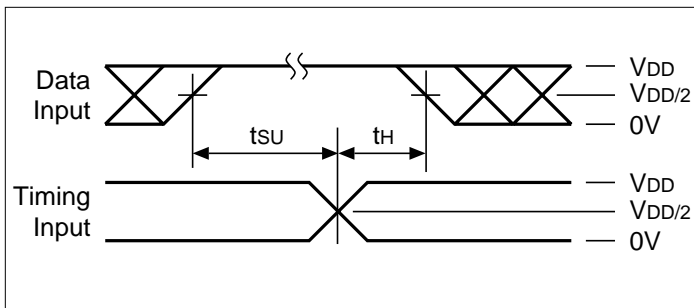
Parameter Measurement Information ($V_{DD} = 1.8V - 3.6V$)



Switch Position

Test	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{DD}$
t_{PHZ}/t_{PZH}	GND

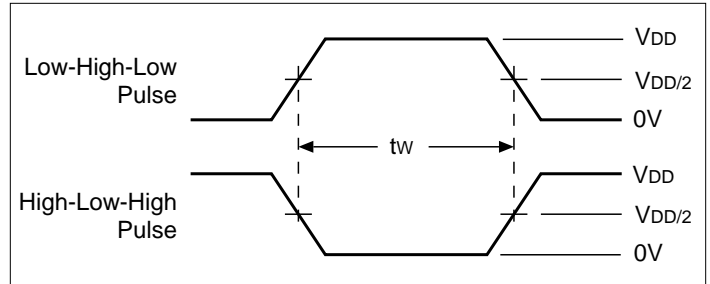
Setup, Hold, and Release Timing



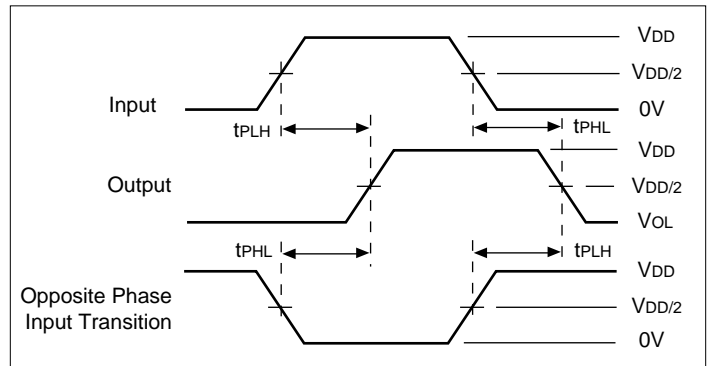
Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:
 $P_{RR} \leq 10 \text{ MHz}$, $Z_O = 50\Omega$,
 $t_R \leq 2\text{ns}$,
 $t_F \leq 2\text{ns}$,
measured from 10% to 90%, unless otherwise specified.
- D. The outputs are measured one at a time with one transition per measurement.

Pulse Width



Propagaton Delay



Enable Disable Timing

